Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] 1. A phase-locked loop circuit comprising:
a voltage controlled oscillator adapted to provide a first clock signal comprising a first frequency; and
a phase frequency detector adapted to compare the first clock signal comprising the first frequency to a reference clock signal comprising a reference frequency, the phase frequency detector comprising a programmable circuit adapted to vary a minimum pulse width of an increment pulse and a minimum pulse width of a decrement pulse, the programmable circuit being further adapted to reduce a static phase error of the phase locked-loop circuit.

[c2] 2. The phase-locked loop circuit of claim 1, wherein the programmable circuit comprises a multiplexer and a plurality of buffers, wherein the plurality of buffers is divided into a plurality of groups, wherein each of the plurality of groups comprises a different number of buffers, wherein each of the plurality of groups is electrically connected to the multiplexer, and wherein the multiplexer is adapted to switch between signals from each of the plurality of groups to vary the minimum pulse width

of the increment pulse and the minimum pulse width of the decrement pulse.

[c3] 3. The phase-locked loop circuit of claim 2, further comprising a digital control signal to the multiplexer to control the switching between the signals from each of the plurality of groups.

[c4] 4. The phase-locked loop circuit of claim 1, wherein the programmable circuit comprises an operational amplifier, a first capacitor, a second capacitor, and a delay line, wherein the operational amplifier is adapted to compare a first analog voltage across the first capacitor to a reference voltage across the second capacitor and generate a control voltage based on the comparison, wherein the control voltage is adapted to control the delay line to vary the minimum pulse width of the increment pulse and the minimum pulse width of the decrement pulse, and wherein the minimum pulse width of the increment pulse and the minimum pulse width of the decrement pulse comprise a fixed fraction of a period of the reference clock signal.

[c5] 5. The phase-locked loop circuit of claim 4, wherein the programmable circuit further comprises an AND gate adapted to extract the minimum pulse width of the increment pulse and the minimum pulse width of the

decrement pulse.

[c6] 6. The phase-locked loop circuit of claim 5, wherein the programmable circuit further comprises a resistor, and wherein the resistor and the first capacitor are collectively adapted to convert a digital signal from an output of the AND gate into the first analog voltage across the first capacitor.

[c7] 7. The phase-locked loop circuit of claim 6, wherein the first analog voltage across the first capacitor is equal to a supply voltage of the phase-locked loop circuit multiplied by the minimum pulse width of the increment pulse and divided by the period of the reference clock signal.

[c8] 8. The phase-locked loop circuit of claim 6, wherein the first analog voltage across the first capacitor is equal to a supply voltage of the phase-locked loop circuit multiplied by the minimum pulse width of the decrement pulse and divided by the period of the reference clock signal.

[c9] 9. The phase-locked loop circuit of claim 4, wherein the reference voltage is generated by a digital to analog converter.

[c10] 10. The phase-locked loop circuit of claim 1, wherein the reference frequency is within a range of about 2 mega-

hertz to about 1 gigahertz.

[c11] 11. A method for reducing a static phase error in a phase-locked loop circuit comprising:
providing a voltage controlled oscillator and a phase frequency detector, the phase frequency detector comprising a programmable circuit;
generating by the voltage controlled oscillator, a first clock signal comprising a first frequency;
comparing by phase frequency detector, the first clock signal comprising the first frequency to a reference clock signal comprising a reference frequency;
varying by the programmable circuit, a minimum pulse width of an increment pulse and a minimum pulse width of a decrement pulse; and
reducing by the programmable circuit, a static phase error of the phase-locked loop circuit.

[c12] 12. The method of claim 11, further comprising:
providing within the programmable circuit, a multiplexer and a plurality of buffers, wherein the plurality of buffers is divided into a plurality of groups, wherein each group comprises a different number of buffers, and wherein each group is electrically connected to the multiplexer; and
switching by the multiplexer, between signals from each of the plurality of groups to vary the minimum pulse

width of the increment pulse and the minimum pulse width of the decrement pulse.

[c13] 13. The method of claim 12, further comprising controlling by a digital control signal, the switching between the signals from each of the plurality of groups.

[c14] 14. The method of claim 11, further comprising:
providing within the programmable circuit, an operational amplifier, a first capacitor, a second capacitor, and a delay line;
comparing by the operational amplifier, a first analog voltage across the first capacitor to a reference voltage across the second capacitor;
generating by the operational amplifier, a control voltage based on the comparison; and
controlling by the control voltage, the delay line to vary the minimum pulse width of the increment pulse and the minimum pulse width of the decrement pulse, wherein the minimum pulse width of the increment pulse and the minimum pulse width of the decrement pulse comprise a fixed fraction of a period of the reference clock signal.

[c15] 15. The method of claim 14, further comprising:
providing within the programmable circuit, an AND gate; and
extracting by the AND gate, the minimum pulse width of

the increment pulse and the minimum pulse width of the decrement pulse.

[c16] 16. The method of claim 15, further comprising:
providing within the programmable circuit, a resistor; and
collectively converting by the resistor and the first capacitor, a digital signal from an output of the AND gate into the first analog voltage across the first capacitor.

[c17] 17. The method of claim 16, wherein the first analog voltage across the first capacitor is equal to a supply voltage multiplied by the minimum pulse width of the increment pulse and divided by the period of the reference clock signal.

[c18] 18. The method of claim 16, wherein the first analog voltage across the first capacitor is equal to a supply voltage multiplied by the minimum pulse width of the decrement pulse and divided by a period of the reference clock signal.

[c19] 19. The method of claim 14, further comprising generating by a digital to analog converter, the reference voltage.

[c20] 20. The method of claim 1, wherein the reference frequency is within a range about 2 megahertz to about 1

gigahertz